



Flows

DESIGN AUTOMATION AND TESTING NEWS
FROM MORGAN KAUFMANN PUBLISHERS



Special Edition: Design Automation Conference

>>> July 24-28 • Moscone Center • San Francisco, CA <<<

Visit Visit Morgan Kaufmann/Elsevier at Booth 814

New Paradigms for On-Chip Communication

Giovanni ("Nanni") De Micheli, Director of the Integrated Systems Center at EPFL, delivered a keynote address at ISCAS in May titled "Systems and Networks on Chips: Challenges and Solutions." The following is an extended abstract of what Nanni discussed.

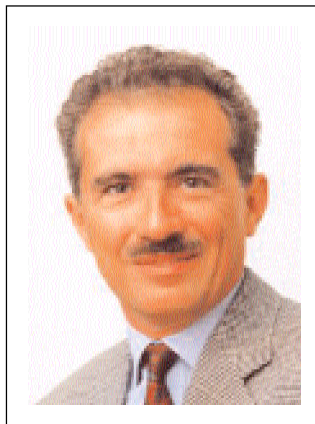
System on Chip (SoC) design faces several challenges which are due to the extremely small nature of electronic devices and the consequent opportunity to realize multi-processing systems of extremely high complexity. To manage large scale design, SoCs are assembled out of complex standard parts, such as programmable cores and memory arrays. Thus, the major design challenge is to provide correct and reliable operation of the interconnected components.

The structured realization of on-chip interconnection is the future platform for multi-processor SoC design, and consists of a micro-network of components, where routing wires can be abstracted as communication channels. Due to device downsizing and voltage downscaling, signal transmission will face an increasingly noisier environment, where noise abstracts undesirable effects such as timing variations, cross-talk and interference.

The design of micro-networks requires the combination of tech-

niques coming from networking and micro-electronic domains.

Design objectives include achieving high bandwidth with low communication latency, low error rates and low energy consumption. Opportunities stem from the ability of using ad hoc networks on chip and designing communication protocols customized to the application and architecture.



Micro-network design can be achieved by extending synthesis technology to cope with the particular features of micro-networks and their components, such as programmable switches, pipelined links and network interfaces to programmable cores and memories. The support for optimization of the network topology and parameters will provide competitive advantage over manual solutions.

Reliable network design will address coping with signal integrity in the physical channels while supporting reliable end-to-end data transmission. Note that signal integrity may be consciously lowered while searching for

Continued on page 4 >>>

NEW! FROM ELSEVIER!

Elsevier and its imprints, Morgan Kaufmann Publishers, Newnes, and Academic Press, are now providing FREE informative newsletters to subscribers.

Newsletter content is driven by you – based on your selected areas of interest.

Newsletters will contain articles written by industry experts, surveys, book reviews, and more!

Simply visit www.elseviernews.com to sign-up!

*Your contact information will not be sold or rented to third parties.

In This Issue

New Paradigms for On-Chip Communication ...PAGE 1

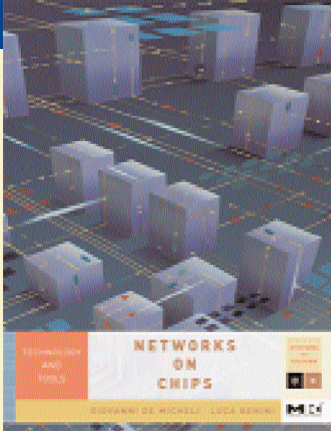
New Books from Industry ExpertsPAGE 2

Reader FeedbackPAGE 3

Authors InvitedPAGE 4

HOT OFF THE PRESS THIS MONTH

Enter offer code 86580 and receive 20% off,
plus free shipping! Offer expires August 31, 2006.



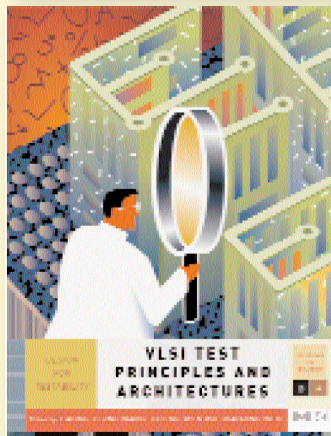
Networks on Chips: Technology & Tools

By Giovanni De Micheli and Luca Benini

Networks-on-Chips are leading edge technology, vital to anyone doing System-on-Chip design!

"This is THE book on Networks on Chips. It covers thoroughly all different levels of abstraction, from circuits to architecture, and covers theory as well as realistic examples." — Wayne Wolf, Princeton University

July 2006 • Hardback • 408 pgs • List Price \$59.95 • ISBN 0123705215



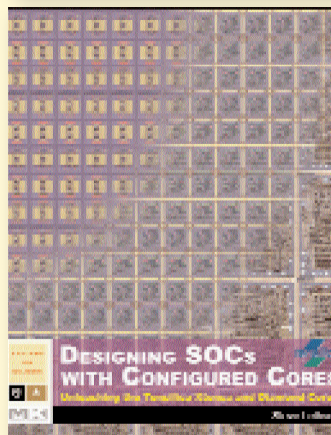
VLSI Test Principles and Architectures: Design for Testability

Edited by Laung-Terng Wang, Cheng-Wen Wu and Xiaoqing Wen

The most up-to-date coverage available of VLSI Testing and Design-for-Testability!

"This is the most recent book covering all aspects of digital systems testing. It is a 'must read' for anyone focused on learning modern test issues, test research, and test practices." — Kewal K. Saluja, University of Wisconsin

July 2006 • Hardback • 808 pgs • List Price \$59.95 • ISBN 0123705975



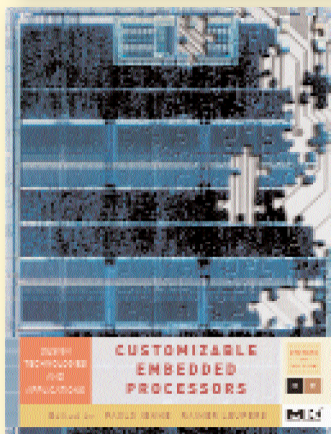
Designing SOCs with Configured Cores: Unleashing the Tensilica Xtensa and Diamond Cores

By Steve Leibson

"This well-written book gives a practical introduction to three basic techniques of modern SOC design: use of optimized standard CPU and DSP processors cores, application-specific configuration of processor cores, and system-level design of SOCs using configured cores as the key building block. Readers will find it is often the first book they reach for in defining and designing their next chip."

— Chris Rowen, President and CEO, Tensilica, Inc.

July 2006 • Hardback • 344 pgs • List Price \$59.95 • ISBN 0123724988



Customizable Embedded Processors: Design Technologies and Applications

Edited by Paolo Ienne and Rainer Leupers

"A new technology called Custom Embedded Processors is fast becoming the key enabling technology of the next 50 years. In this book the reader will learn the basic theory, and practical examples of how this powerful new approach has been put to use. It's a must read for anyone hoping to build the next big thing in the 21st century." — Alan Naumann, President and CEO, CoWare, Inc.

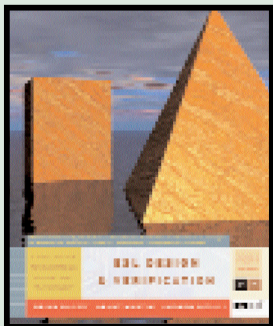
July 2006 • Hardback • 528 pgs • List Price \$59.95 • ISBN 0123695260

ORDER ONLINE! www.mkp.com

ESL Design and Verification

A Prescription for Electronic System Level Methodology

Brian Bailey, Grant Martin, Andrew Piziali. With contributions by: M. Burton, J. Greenbaum, K. Hashmi, A. Haverinen, L. Lavagno, M. Meredith, B. Murray, I. Oliver, C. Passerone, J. Sanguinetti, and F. Schaefer



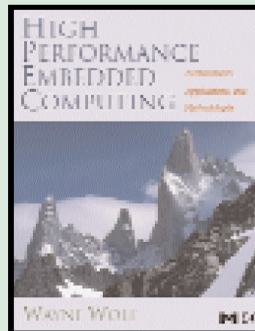
ESL is evolving into a set of complementary methodologies that enable embedded system design, verification and debug through to the hardware and software implementation of custom SoC, system-on-FPGA, system-on-board, and entire multi-board systems. This book

arises from experience the authors have gained from years of work as industry practitioners in the Electronic System Level design area; they have seen “SLD” or “ESL” go through many stages and false starts, and have observed that ESL seems to be really happening – the shift in design methodologies is occurring.

Coming in time for DATE 2007
\$59.95 • ISBN 0-12-373551-3

COMING SOON!

High-Performance Embedded Computing



Architectures, Applications, and Methodologies

By Wayne Wolf

“This book has much to contribute. More and more embedded devices are becoming available, with people walking around with cell phones, PDAs, and MP3 players. The design and constraints of these devices is quite different from a generic computing system such as a laptop or desktop PC. This book provides an abundance of information on these basic design topics while also covering newer areas of research such as sensor networks and multiprocessors.”

— Mitch Theys, University of Illinois

Sept. 2006 • \$69.95 • ISBN 0-12-369485-X

“Anant Agarwal, Professor at MIT and co-author of *Foundations of Analog and Digital Electronic Circuits*, poses questions about the future of digital and analog circuits. WE’D LOVE TO KNOW WHAT YOU THINK!”

Answer these brief survey questions and receive 30% off one of the titles featured in this newsletter, plus free shipping!

One person will win a digital camera!*

Respond by answering: **A STRONGLY AGREE** **B AGREE** **C DON'T CARE**
D DISAGREE **E STRONGLY DISAGREE**

- | | |
|---|---|
| <p>1 Analog circuits and electronics concepts are extremely relevant in today's industry. _____</p> <p>2 Our advanced courses in EE and ECE adequately prepare our students for today's job market. _____</p> <p>3 Our introductory courses in circuits and electronics adequately prepare our students for advanced courses in EE and ECE and today's job market. _____</p> <p>4 Introductory circuits and electronics courses and textbooks need rethinking to reflect contemporary technologies and practices. _____</p> | <p>5 Analog and digital electronics should be combined into a single introductory course in the EE and ECE curriculum. _____</p> <p>6 The MOS transistor should replace the BJT in introductory circuits and electronics texts. _____</p> <p>7 In your opinion, what percentage of the examples in an introductory EE course in circuits should be motivated by digital or VLSI applications? (Circle One).</p> <p>0% 25% 50% 75% 100%</p> |
|---|---|

Send your answers and contact information to e.newsletter@elsevier.com

We will randomly select a winner on August 31st. *No purchase necessary. Survey questions must be received by Elsevier by August 30th to be eligible to win. Odds of winning digital camera: 1:7,500.

See Anant's upcoming article on this topic in the fall edition of *FLAWS*.

operational voltages of computational/storage units and voltage swings on links that reduce the system energy consumption.

Information encoding, packetization and routing are distinctive aspects of reliable micronetwork design.

Information encoding in switches or data interfaces has shown to be effective in raising the mean time to failure (MTTF) of communication links in noisy environments. Shadow registers have been successfully used to increase resiliency against soft errors, and more generally, against timing errors.

Data packetization provides us with a versatile framework to encapsulate data for reliable transmission with a low overhead. Different packetization schemes and packet routing strategies have also been addressing specific needs for micro-networks, such as the support for guaranteed throughput on specific

links in combination with best-effort communication services on other links.

Overall, the design of reliable micronetworks is a challenging research area. The combination of various design objectives, such as performance, low-energy communication, and MTTF addresses some of the current needs of the design communi-

For an in-depth analysis of all the on-chip communication challenges, read Nanni and Luca's new book, *Networks on Chips*. See page 2 for details...

ty. Moreover, the ability to synthesize and optimize reliable micro-networks provides a competitive advantage for the realization of complex multi-processor SoCs.

This plenary talk surveyed the area of System on Chip design, with particular reference to the challenges provided by the 65 and 45 nanometer node technology, as well as by novel silicon (and non silicon) -based technologies. New and future design styles and methodologies were presented, with an eye on the medium and long term technology trends.

AUTHORS INVITED

If you are planning to write a book in the near future, please consider Elsevier your best option as publisher!

Elsevier publishes books under the Morgan-Kaufmann, Academic Press, and Newnes imprints. You will see books from each of these imprints at this exhibit.

If you would like to submit a book proposal, or have any questions about our publishing program, please contact us:

.....
Charles B. Glaser
Senior Acquisitions Editor
c.glaser@elsevier.com

INSTRUCTORS:

Some Elsevier books are available for course adoption.

Register to request a review copy online at www.textbooks.elsevier.com or email your complete contact details with course information to textbook@elsevier.com.



30 CORPORATE DRIVE
SUITE 400
BURLINGTON, MA 01803

PRESORTED
STANDARD
U.S. POSTAGE
PAID
ELSEVIER