The Role Of Verification at the Architectural Definition Stage (and Beyond.)

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The SoC Verification Problem:

• When the system is on a chip, verification includes:
  – Hardware function
  – Software function
  – Performance of hardware + software

• Architects need a platform for analyzing hardware/software tradeoffs as well as system and component performance.

• Embedded software engineers need a platform for early software development.

• Verification engineers need a platform for early test development.
The Solution: A methodology, tools and models to support simulation from the transaction-level down to RTL

<table>
<thead>
<tr>
<th>Model Application</th>
<th>Model Type</th>
<th>Model Attributes</th>
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<tbody>
<tr>
<td>Embedded S/W Development</td>
<td>ISS + TLM Blocks</td>
<td>High Performance</td>
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<tr>
<td>Directed Hardware Performance</td>
<td>TLM Blocks + Stochastic Stimulus Generators + Analysis Tools</td>
<td>High Turn Around Time (Fast &amp; Highly Configurable)</td>
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<tr>
<td>S/W + H/W Performance Estimation</td>
<td>ISS + Cycle-Accurate</td>
<td>High Accuracy</td>
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ISS: Instruction Set Simulator (fast CPU model)  TLM: Transaction-Level Model
Functional Virtual Prototype: Reuse TLMs and Stimulus Generators in RTL Verification

- Early embedded SW
- Early performance evaluation

- Final embedded SW
- Final functional verification