Verification requires new methodologies, panelists say

By Richard Goering
EE Times
February 02, 2005 (10:40 PM EST)

SANTA CLARA, Calif. — There's no silver bullet that can solve the design verification problem, said participants in a plenary panel at the DesignCon conference here Wednesday (Feb. 2). There are tools that can help, panelists said, but the real issue is rethinking the methodology.

The panel was convened to look at the full span of IC verification, from functional through physical verification. Moderator Sergio Camerlo, director of engineering for interconnects and packaging at Cisco Systems, noted that the verification effort is often overlooked and underestimated. His question to the panel: How do we go from specification to closure?

Dhrumil Gandhi, vice president of product technology at ARM Ltd., said that the use of intellectual property (IP) building blocks is a necessity. Blocks must be both pre-verified and verifiable in the system-on-chip (SoC) environment, he said. Issues for IP verification, he said, include model-to-silicon correlation, manufacturability, design margins, and sensitivity analysis.

"At ARM, we find all the bugs we can," Gandhi said. "There is no such thing as correct by construction design. You have to have measurable verification — that's the only way we can control the verification task."

Yaron Kashai, vice president of research and strategic technology at Verisity, quoted a 1998 Nortel study that showed verification takes up most of the design cycle — even with a "mediocre" success rate with respins. Since then, Kashai said, there have been a number of new tools, several new languages, and new approaches like coverage-driven verification and assertion-based verification.

"Did it make a difference? In my mind it did, but the verification problem grew. We're fighting the curve of complexity," Kashai said. His prescription: plan ahead, know your tools and methods, and measure and improve the process.

Next-generation designs need to go beyond IP reuse, said Sudhakar Sabada, vice president for design technology at LSI Logic Corp. What's needed, he said, are configurable design platforms, early system integration, improved off-the-shelf IP quality, and the linking of design and manufacturing. Process sensitivity needs to be accounted for, he said, and statistical analysis will be a "key requirement" going forward.

Joe Sawicki, vice president and general manager of Mentor Graphics' design-to-silicon division, focused his remarks on physical verification. He noted that physical verification tools face a number of new manufacturability challenges, and that they must cope with issues like metal slotting, metal fill, and rule and model-based optical proximity correction (OPC).

The problem with foundry-recommended design for manufacturability (DFM) design rules, he said, is that a user could end up with thousands of potential violations. "We have to go to a viewpoint that's more statistical. Rather than a yes or no, we have to give you data about your design," he said.

Ronnie Vashista, vice president for marketing at eASIC Corp., observed that it's impossible to have 100 percent functional regression coverage, and that first-time silicon success won't always happen. The antidote, he said, is a way to go from RTL to volume ASIC chips in one month, so designers can run a full system-level verification.

Speaking from the audience, consultant Brian Bailey asked if anything is being done to change the design process so there's less need for verification.

"There are flows we apply so the probability of bugs is reduced," said ARM's Gandhi. "Well defined interfaces and design rules at a high level help make sure the design conforms to the intent we started out with."

"To some extent, you can design things so they're less buggy, but it's an elusive concept," warned Verisity's Kashai. "People who try to just design and ignore verification don't make it."

The verification process itself needs to be well thought out and measurable, Kashai said. LSI's Sabada agreed. "You need to have a methodology," he said. "Just because you have tools doesn't mean you'll have success."